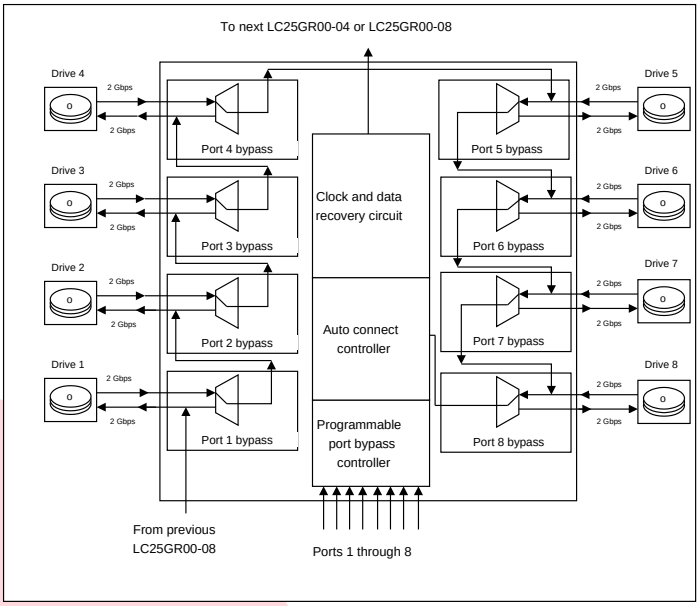
LC25GR00-04/-08

The PHY-er-Chip R

LC25GR00-04/08

Advance Product Information



Block Diagram

FEATURES

GENERAL

2.5Gbits/Sec Fiber Channel Repeater

4/8-port Repeater with daisy chain link

Optional Advance PRML data and clock recovery

Maximum data jitter of 70p.S.

Maximum propagation bypass delay of 3.0 n.S.

Exceed MJS-10 specification performance

Lowest power consumption at 2.5Gb/S, 550mW max

Fully compliant with ANSI-X3T11 Fiber Channel Specification

Fully scalable technology path toward 10Gb/S

Programmable Intelligent Bypass and auto- connect controller

Advance 0.18microm CMOS technology

84-pin or 100-pin PQFP package