

**Super HDD Processor, Integrated Hard Disk Controller, ARM7TDMI, Servo Logic,
Buffer Memory, Data Memory and IDE/PCMCIA Interface.**

CPU

- ARM7TDMI 32-bit RISC processor
- Embedded ICE through dedicated JTAG port
- JTAG may be multiplexed with other signals though enable pin

PCMCIA ATA Interface Block

- PCMCIA memory and I/O mode
- ATA pass-through mode
- PIO modes 0, 1, 2, 3 and 4
- DMA modes 0, 1 and 2
- Auto write/read command execution

ECC Block

- Hardware triple-burst on-the-fly detection and correction
- 224-bit Reed Solomon code

Disk Controller

- Headerless Architecture requires no tables
- Supports up to 300 Mb/s R/W channel bit rate
- Defect FIFO

Internal Memory

- 16K x 32-bit internal buffer SRAM
- Zero-wait state
- Byte-write capability

Flash Controller

- 8-bit Serial Flash interface
- Programmable interface timing

Interrupt Controller

- Prioritized interrupts
- Vectored interrupt control for fast ISR entry

Memory Access Controller

- 16K x 32-bit internal buffer SRAM
- Host channel with 32-byte FIFO
- Disk channel with 32-byte FIFO
- Independent host auto-read and auto-write pointers
- Data Flow Control
- Byte-write from CPU

Servo Interface

- Four Burst or Customer defined

Motor Control

- Speed error determination through spindle feedback

Synchronous Serial Interface

- Dedicated 1-bit servo burst data acquisition serial interface (if supported by channel)
- Three 3-bit serial interfaces

Power Management

- Power levels
- Automatic CPU wake on interrupt
- Interfaces independently tri-statable
- Automatic read channel wake/sleep

UART (Optional)

- 2-wire interface
- 16450 register interface

Timers

- General purpose timer
- Three timeout modes
- Watchdog Timer
- Watchdog may be used as second general purpose timer