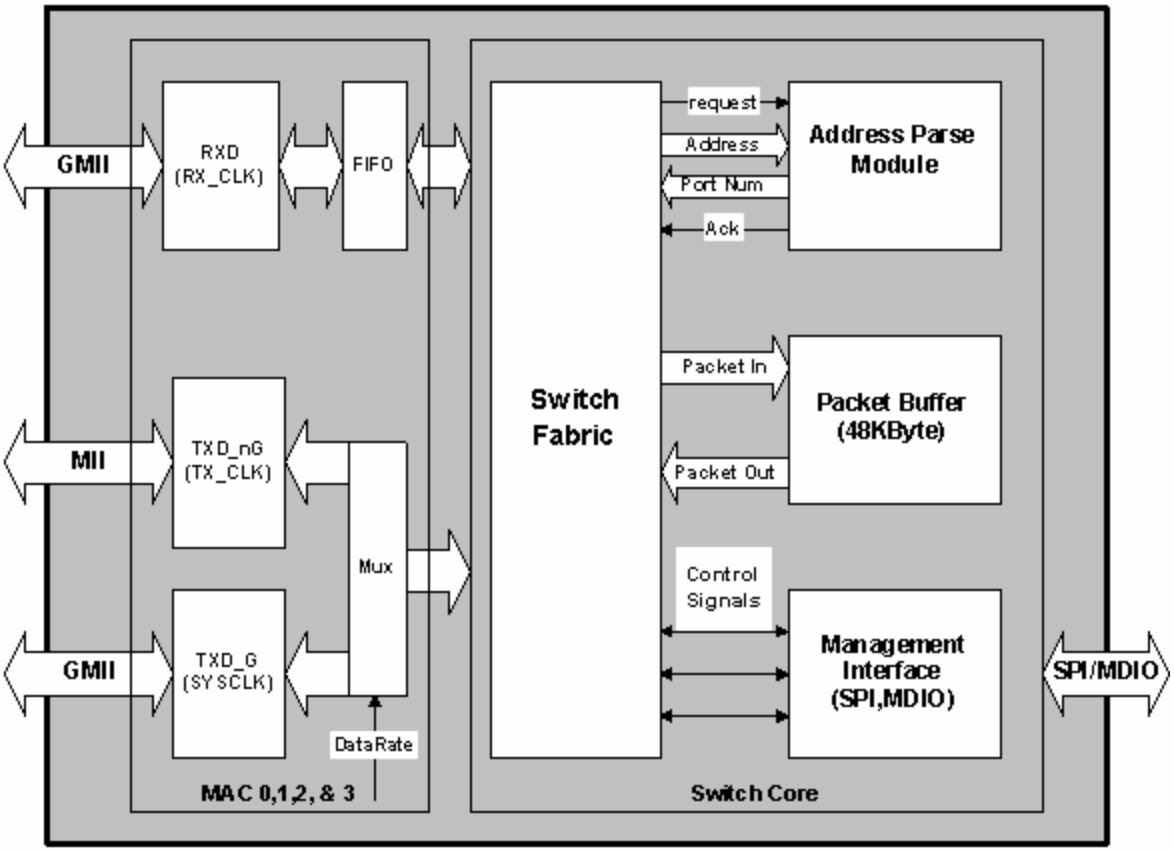
DESCRIPTION

This Layer 2 Switch provides an ideal solution for the design of unmanaged full wire-speed multi-port Gigabit Ethernet (GbE) switches. Each port supports either 10/100/1000Mbps data rate. Flow controls, backpressure in half duplex mode and PAUSE frame in full duplex mode are employed to solve the HOL (Head of Line) blocking.

This Layer 2 Switch integrates four half/full duplex mode 1000BASE Gigabit Ethernet MACs, wire speed switching engines, MAC address based Address Parsing Algorithm, Packet buffer memory.

FEATURES

- Supports four 10/100/1000 Mbps Ethernet ports with GMII/MII interface.
- IEEE 802.3ab CSMA/CD Compliant
- Full and half duplex mode of operation.
- Speed and Duplex mode auto-negotiation through MDIO.
- Self address learning mechanism supports 512 MAC address.
- Automatic address aging with 300 seconds default.
- 1Mbit packet buffer memory embedded
- SPI interface employed to communicate with MCU.
- IEEE802.3ab flow control for full duplex operation.
- Supports Store-and-Forward mode of operation.
- 0.18 micron, 1.8V CMOS technology packaged in 160-pin PQFP.
- 3.3V I/O.



Ethernet Level 2 Switch Block Diagram