1. LDV5010 FEATURE OVERVIEW

The LDV5010 Channel is tailored to run on the 41.85MHz Digital Video Camera (DVC) platform. The main function is to read the signal from the media (presented by the preamp), extracting the data and the data clock for the controller. The secondary function is to detect the Automatic Tracking Frequencies of 465KHz and 697.5KHz. In the DVC system, the LDV5010 interfaces to the Preamp, MicroProcessor and Controller. Channel performance information is available through LDV5010's Quality Engine, which can be used as a metric to help optimize the channel's bit-error-rate.

The LDV5010 utilizes a 0.18 micron CMOS process technology for low power consumption and a small die area. The part requires two power supplies: 3.3V +/-10% and 1.8V +/-10% or one power supply of 3.3V +/-10% (with internal 1.8V voltage regulator enabled). The part is available in a 64-pin TQFP package.

2. CHIP FEATURES

2.1. General Features

- Fully integrated 41.85 MHz Read Channel Device
- Supports constant density recording of 41.85Mbps with no external component changes
- Fabricated in .18 micron CMOS technology
- Operating supply voltages: 3.3 ± 10% and 1.8 +/-10% volts or one 3.3 ± 10% (with internal 1.8V voltage regulator enabled).
- Available in a 64-pin TQFP package.

2.2. Read Data Conditioning

- Full-Differential Analog Front-End
- PR4 Automatic Sampled-time Gain Control Loop Algorithm
  - 4-Banded Variable Gain Amplifier to accommodate input signal ranges of 30-300mVppd
  - normalize the incoming data within 100-300 samples
  - Optional VGA initial gain shadow registers for each head/field combination
  - Locks to random or 6T acquisition fields
- 7^{th}-order Bessel Continuous Time Filter
  - Programmable Filter Supports Cut-offs from 6 to 30 MHz
  - Filter boost programmable from 0 to 10dB
  - Flat Group Delay +/- 5% up to 1.5* Fc, without boost
- 6-bit Analog-To-Digital Converter
  - Automatic Offset Correction
- PR4 Sampled-time Timing Recovery Loop to frequency and phase acquire
  - acquires to the incoming data within 100 to 300 samples on a 6T acquisition field
  - Locks to random data or a 6T acquisition field
- Digital Full-LMS Adaptive Equalizer
  - Correlation Detector detects highly correlated fields (2T, 4T, 6T or 12T) and stops adaptation

- PR4 Viterbi for Data Detection
- Programmable Drop-Out detection

2.3. User programmable fields for system optimization

- Programmable Head Recovery Delay
- Programmable IDLE times after drop-out, excess zeros and gaps
- Programmable Length of LowZ after readgate (RG Pin) assertion
- Programmable acquisition field lengths for gain and timing recovery loops

2.4. Head and Field Sensitive Features

- When applicable, unique user defined parameters are provided for audio, and non-audio fields for head0 or head1 combinations in order to optimize for each head/field combination.

2.5. ATF Detector

- The LDV5010 includes a Digital Heterodyne Tuner to detect the servo automatic tracking frequencies (ATF)
- Servo tone amplitude difference is provided on the STDIF output pin.

2.6. Trick Mode Support

- Due to the programmable registers, the user is able to configure the part to work properly in various modes of operation, such as NTSC LP Forward and LP Reverse.
- Dropouts are automatically detected via the Dropout detector block

2.7. Channel Optimization Vehicles

- Quality Metrics for use in Channel Optimization
- 8-bit Digital Test Bus for Testability and Channel Optimization

2.8. Test Modes

- Built-In-Test logic to minimize test vectors and allow fault testing in the field
- Analog Test Inputs and Outputs are provided for control and observation of internal analog blocks
- An 8-bit Digital Test Bus is provided for Digital and some Analog Testability

2.9. User Interface

- Three-bit Serial Interface Port for access of internal configuration registers
  - to load and verify register contents
  - to monitor status
  - to collect chip feedback

2.10. Powerdown Modes

- Register controlled powerdown of analog blocks
- During non-read mode, the clock to the digital logic is shut-off to conserve power

- An internal Power-On-Circuit (POR) monitors the voltage level. When the voltage is too small, the chip is placed in powerdown mode, until the voltage assumes a working level.
- External Power-down pin

3. ABSOLUTE MAXIMUM RATINGS

Input Voltages:

CMOS Digital Pins..... .... -0.3 V +3.6 V
Analog Pins..... .... -0.3 V +3.6 V
Storage Temperature, T_{stg}.... .... -65°C to 150°C
Junction Temperature, T_J.... .... 0 °C to 110°C

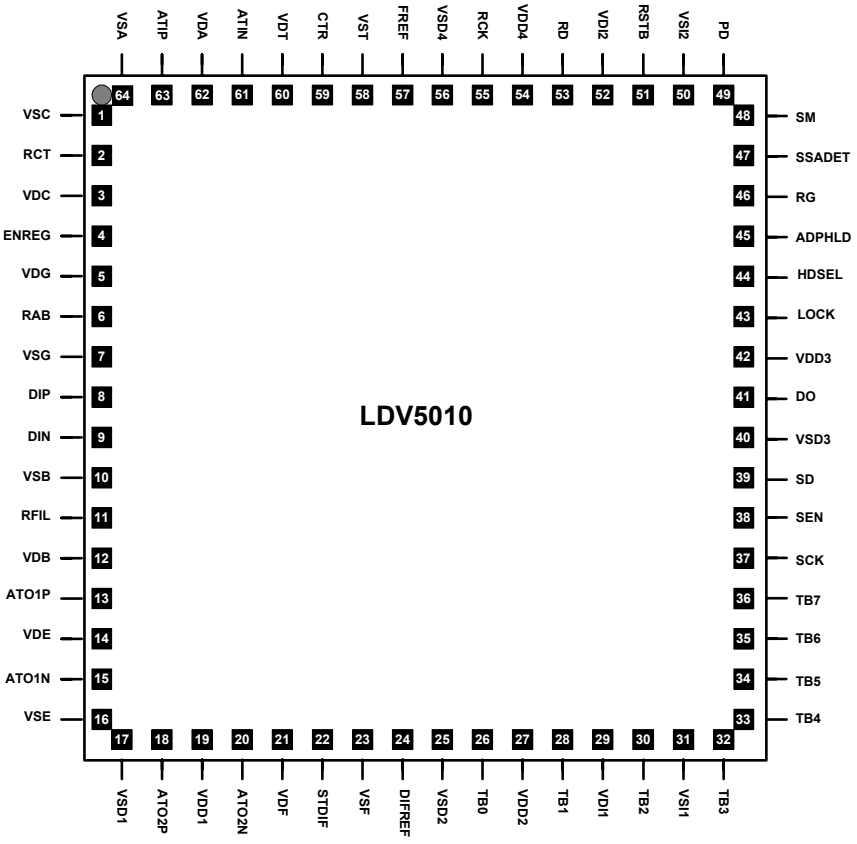
Thermal Impedance, Θ_{JA}:

Still Air..... .... 51°C/W
200 fpm air flow..... .... 38°C/W
600 fpm air flow..... .... 27°C/W

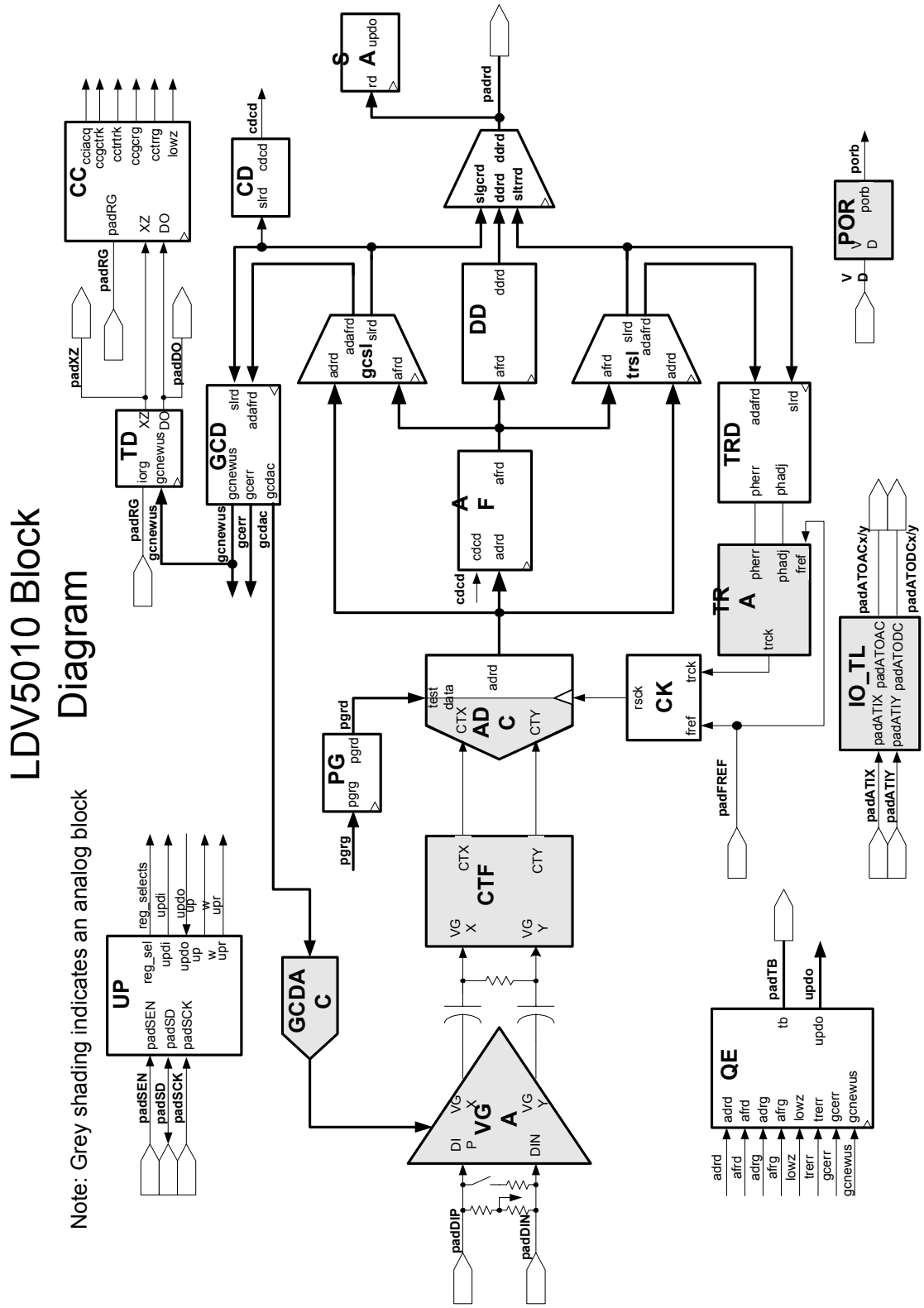
Maximum power consumption:

Power supply maximum drawn current (with internal 1.8V regulator enabled @V_{CC} = 3.3V)..... ..... 70mA

4. LDV5010 CHIP I/O



Pin assignments for LDV5010 in a 64-pin TQFP package.



LDV5010 Data Path Block Diagram